IN THE SPECIFICATION:

Kindly replace paragraph 7 on page 1, with the following:

[7] As is shown in Fig. 1, a typical disk drive system includes a hard disk controller (HDC) 12 that interfaces with a R/W channel or RDC 14 which is in communication with a disk 16. Data transfer between HDC [[22''']] 12 and the R/W channel is synchronized by read gate (RGATE) and write gate (WGATE) control signals. In a read operation, R/W channel 14 processes an incoming analog signal from disk 16 and transfers the data to HDC 12. In a write operation, data is transferred from HDC [[22''']] 12 to the R/W channel to be written to the disk. Latency refers to the time or byte delay that data remains in the R/W channel. Some disk drive systems have latencies of about 20 bytes which, depending on the particular system, amounts to a time delay of between about 800 ns and 5 ms.

Kindly replace paragraph 73 on page 9, with the following:

[73] Interface 20 also comprises an RCLK signal sourced by R/W channel 24 having a constant width of 8 times R/W channel [[24''']] 24 clock and an WCLK signal sourced by HDC 22 having the same clock frequency as RCLK but at a different phase.

Kindly replace paragraph 77 on page 10, with the following:

[77] Each of HDC [[22''']] 22 and the R/W channel 24 include appropriate circuitry for transmitting and receiving the various signals, data and mode selection information between the two hardware components. For example, HDC 22 includes a R/W transmit circuit 60 that transmits the R/W signal to R/W receiver circuit 32 on R/W channel 24, a data valid transceiver circuit 64 that transmits the DATA_VALID signal to and receives the DATA_VALID signal from a data valid transceiver circuit 36 on R/W channel 24. A ready

transceiver 66 is provided in HDC [[22''']] 22 to transmit HDC_RDY signal to and receive RC_RDY signal from a ready transceiver circuit 38 on R/W channel 24. HDC 22 also comprises a RWGATE transmit circuit 68 which transmits the RWGATE signal to RWGATE receive circuit 40 of R/W channel 24. HDC 22 also includes a write clock transmit circuit 74 to transmit the WCLK signal to write clock receive circuit 46 on R/W channel 24. HDC 22 comprises a SM transceiver 76, which transmits the SM_DET or SM_ST signal to and receives the SM_DET or SM_ST signal from the SM transceiver 48 on R/W channel 24. HDC 22 and R/W channel 24 comprise respective NRZ transceivers 78 and 50, respectively, for exchanging NRZ data and serial transceivers 82 and 54 respectively for exchanging serial data. R/W channel 24 comprises a buffer full transmit circuit 34 to transmit the BUF_FULL signal to a buffer full receive circuit 62 on HDC 22, a receive clock transmit circuit 44 to transmit RCLK signal to a receive clock receive circuit 72 on HDC 22. R/W channel 24 comprises done transmit circuit 52 to transmit the RDONE or WRITE done signal to done receive circuit 80.